

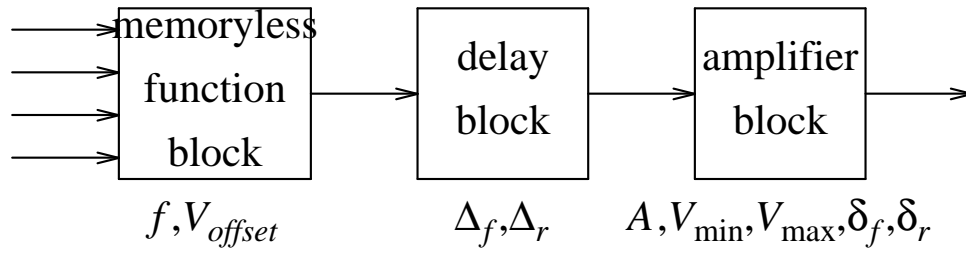
Simulating Continuous Systems with Piecewise-Linear Signals using Time Warp

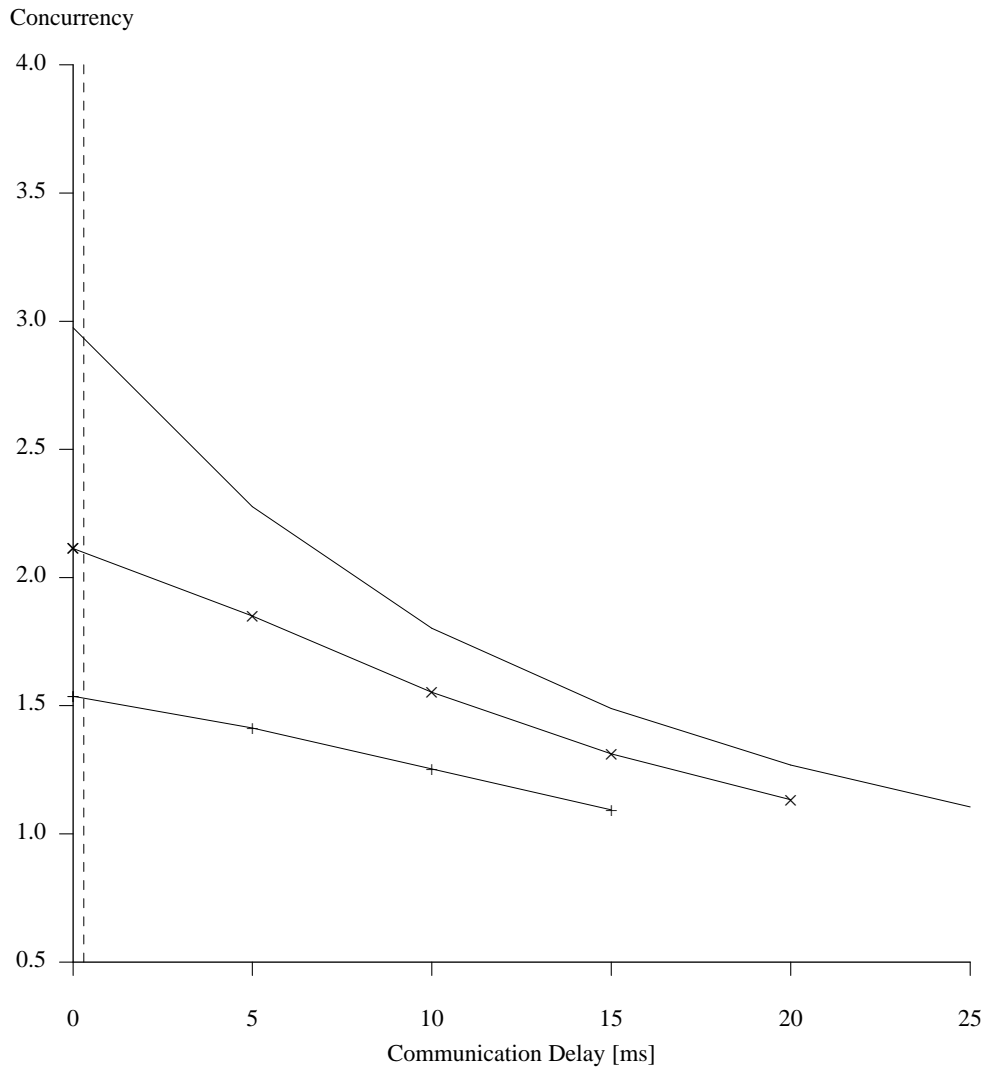
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Basic Component Model



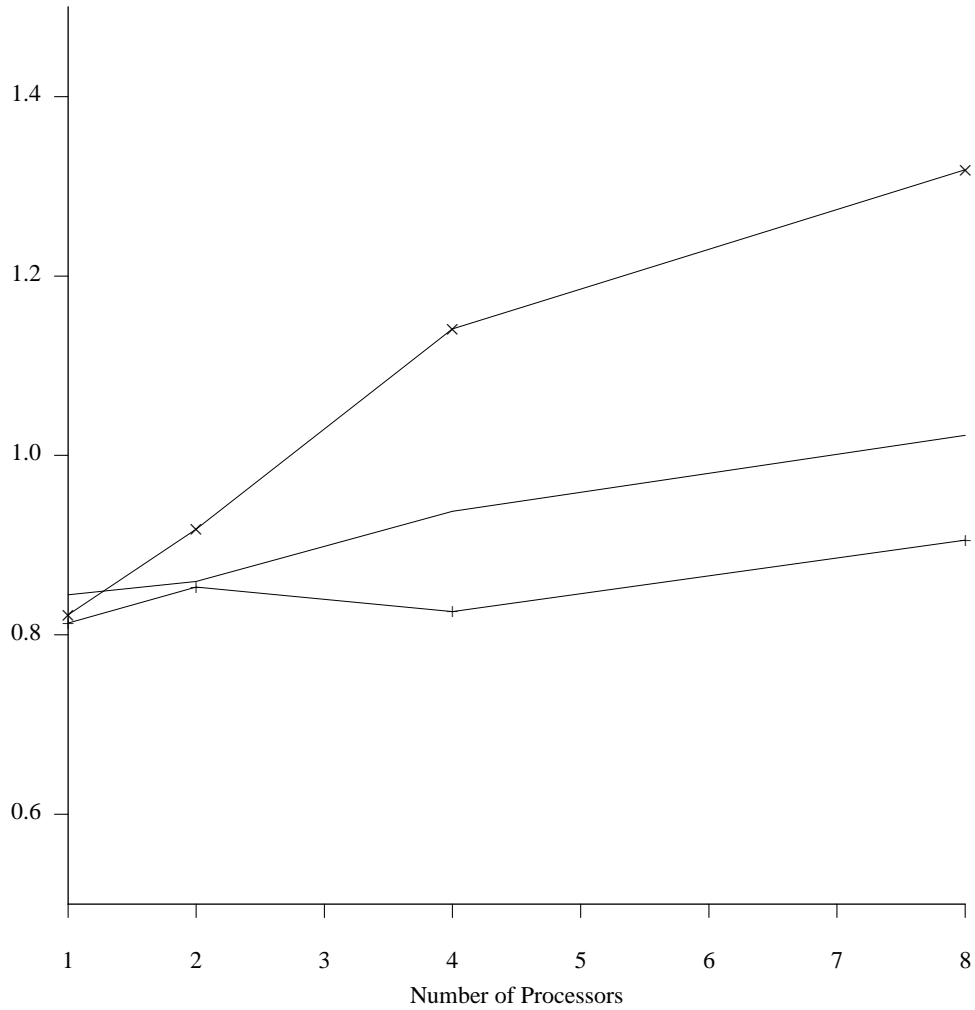


Legend:

- + — + number of processors=2
- x — x number of processors=4
- number of processors=8

Detected Concurrency vs. Communication Delay, 8-bit analog-to-digital converter, state-saving overhead=0.

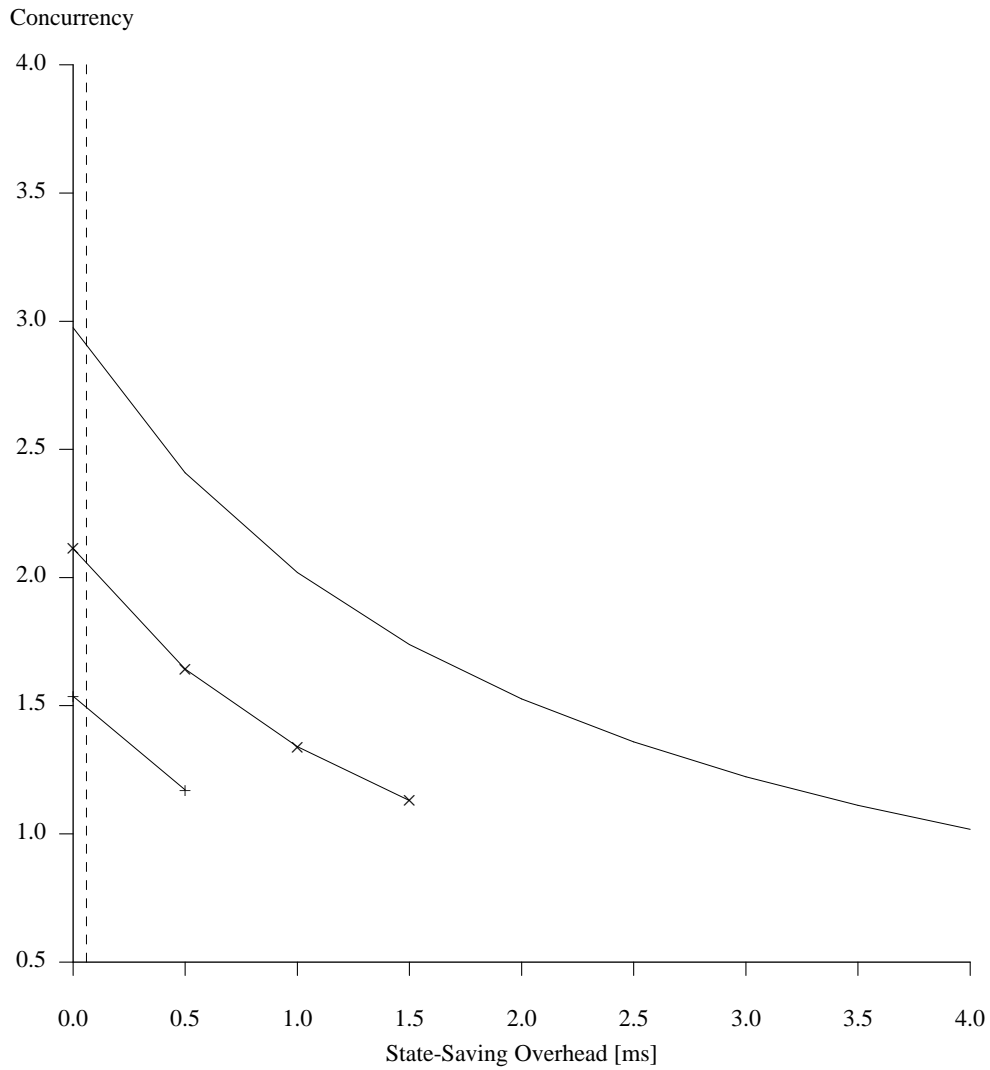
Efficiency



Legend:

- + — + 4-bit synchronous counter
- x — x 4-bit asynchronous counter
- 8-bit analog-to-digital converter

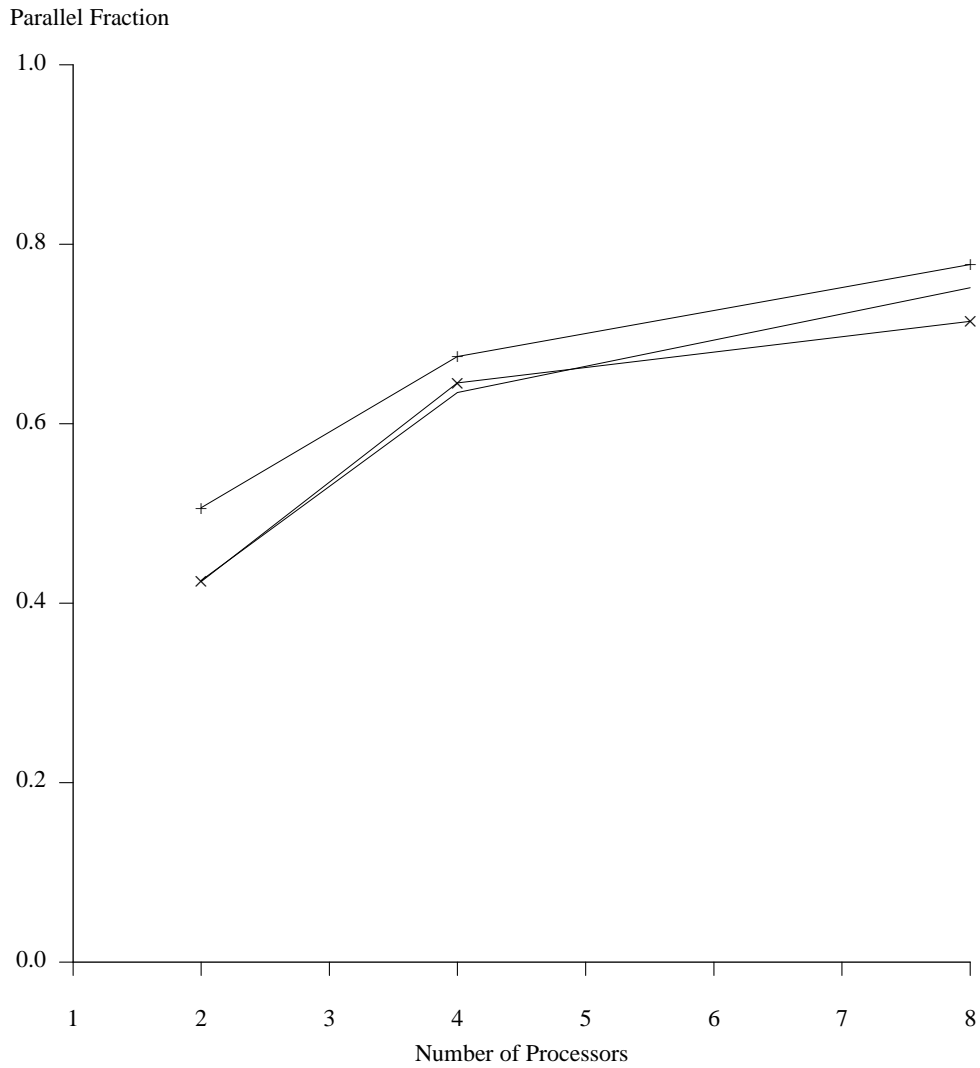
Efficiency vs. Number of Processors, lazy cancellation, MMT scheduling.



Legend:

- + — + number of processors=2
- × — × number of processors=4
- number of processors=8

Detected Concurrency vs. State-Saving Overhead, 8-bit analog-to-digital converter, communication delay=0.

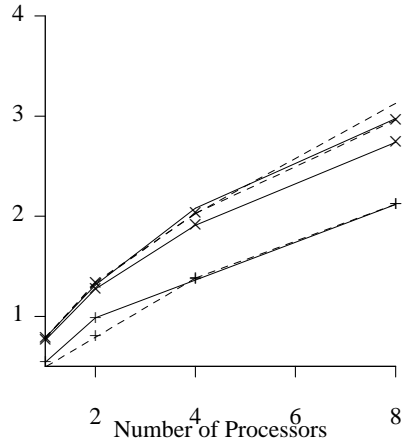


Legend:

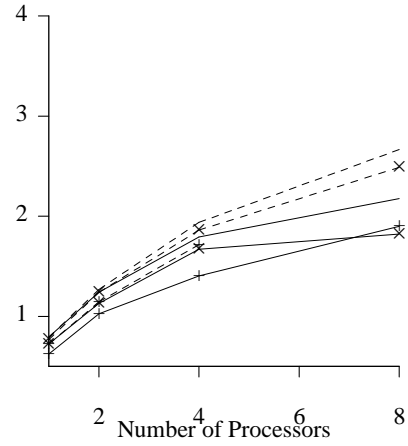
- + — + 4-bit synchronous counter
- × — × 4-bit asynchronous counter
- 8-bit analog-to-digital converter

Parallel Fraction vs. Number of Processors, lazy cancellation, MMT scheduling.

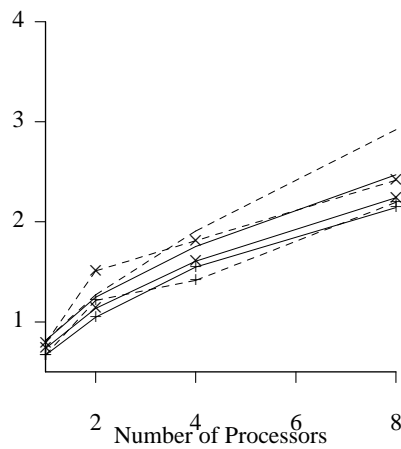
Speedup, Synchronous Counter



Speedup, Asynchronous Counter



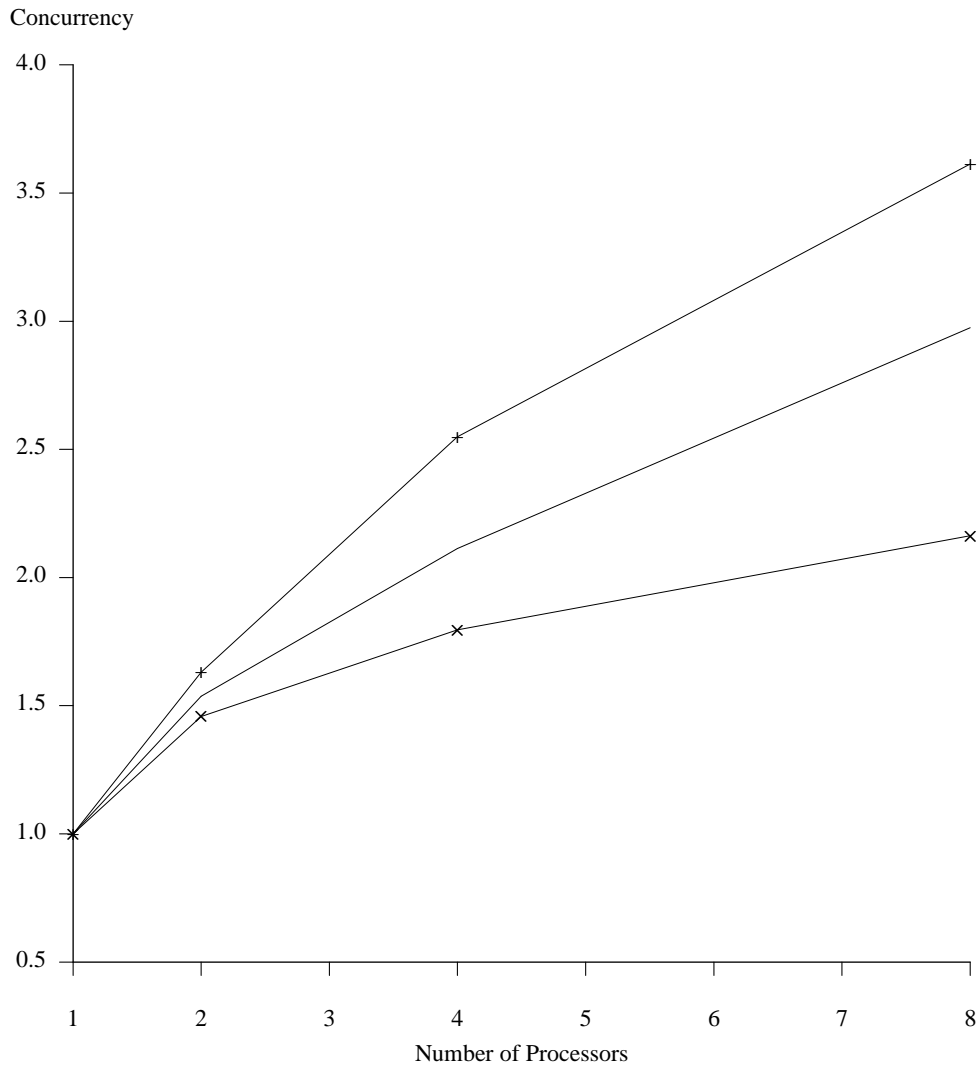
Speedup, A/D Converter



Legend:

- + — + aggressive cancellation, RR scheduling
- x — x aggressive cancellation, MVT scheduling
- — — aggressive cancellation, MMT scheduling
- + - - + lazy cancellation, RR scheduling
- x - - x lazy cancellation, MVT scheduling
- - - - lazy cancellation, MMT scheduling

Speedup vs. Number of Processors.



Legend:

- + — + 4-bit synchronous counter
- x — x 4-bit asynchronous counter
- 8-bit analog-to-digital converter

Detected Concurrency vs. Number of Processors.